Please replace the previous BACKGROUND OF THE INVENTION with the amended one provided below.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to an analysis of a waveform for a telecommunication system or for a measurement equipment, and more particularly to a Digital Signal Processing of Multi-Sampled Phase (DSP MSP).

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems and for a wide range of data rates and waveform timings.

The invention further includes Sequential Data Recovery from Multi Sampled Phase (SDR MSP), which is a version of the DSP MSP, which provides clock and data recovery for optical communications.

Background Art

~~Present~~ Conventional waveform analyzers and serial data receivers use an analog front end for signal filtering, data recovery, and for a generation of data recovery sampling clock.

Therefore more expensive bipolar or BICMOS technologies are needed to achieve sufficient performance, and said present designs have rather limited noise filtering capabilities and are able to cover only narrow application areas.

Analog design problems are further compounded by lower supply voltages which cause insufficient voltage head-room in deep sub-micron IC's which are becoming dominant in today's and future electronics.

There was a need for a waveform timing analyzer and a digital method of signal analysis which will reduce cost and complexity by replacing said analog or BICMOS technologies with less

expensive CMOS technologies, and will improve noise filtering and increase programmability of data analysis algorithms and improve reliability of data recovery functions.

~~Background art for this invention is represented by the documents listed below:~~

~~D1 (US 5,668,830 by Georgiu Christos John ET AL)~~

~~D2 (PCT/CA01/00723 invented by Bogdan);~~

~~D3 (US 2002/0009171 invented by Ribo);~~

~~D4 (US 5,592,125 invented by Williams);~~

~~D5 (US 6,987,817 invented by Reuveni)~~

~~The D1 is limited to using delay lines and most basic digital filters for removing phase noise of waveform edges. D1 circuits enable merely edge phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only.~~
~~Consequently, D1 circuits do not have any of the fundamental features of the present invention such as; over-sampling and noise filtering from entire pulse necessary for elimination of noise occurring inside data pulses, or cumulative processing operations necessary for measuring and processing lengths of transmitted pulses, or adaptive signal processing using wave-form screening.~~

~~The D2 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits. However these D2 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing. Therefore besides said high resolution phase capture, the D2 solution has fundamentally different principle of operation and produces entirely different results.~~
~~Consequently D2 can not contribute to any processing of much higher frequency signals commonly used in communication links.~~

~~The D3 solution represents latest generation of clock and data recovery (CDR) circuits which~~

~~over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.~~

~~The D3 captures windows consisting of samples covering entire data bit interval.~~

~~Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.~~

~~Therefore the D3 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.~~

~~Obviously such window centering can only be achieved by phase locking to the received signal.~~

~~Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD) represented by D4.~~

~~While taking more samples provides D3 with better base for jitter filtering than that of the CDR with BBPD, dynamics of D3 phase locking has to accommodate additional interference caused by said jiter filtering and by further processing of output data providing return reference for the D3 phase locked loop.~~

~~Similarly as the D3 and the CDR with BBPD, all other conventional analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to received signal in order to recover data based on sampling localized in a credible region of the received wave-form.~~

~~The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:~~

- ~~Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.~~
- ~~Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.~~
- ~~Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of~~

~~data links.~~

~~Still other over-sampling solution is described in D5 as designed originally for processing serial data streams from a recordable medium like CD or DVD. Nevertheless some of D5 teachings describe data recovery circuits, which derive number of data bits received in a waveform pulse by dividing a length of the pulse by a bit widths calculated statistically by processing received signal wavefroms. Such pulse lengths is calculated originally as a sum of all oversampling sub-clocks occurring during the pulse, and is divided by such statistically calculated bit width later on.~~

~~However such calculations of the sub-clocks sum and such divisions involving long pulses, limit data rates which D5 solution can be utilized at. Furthermore limited accuracy of such statistically calculated bit widths and division error accumulated during any long pulse processing, increase error rates and limit reliability. Still furthermore; since such statistical processing of the bit widths is performed in a closed loop, it can cause stability problems due to highly unpredictable phase noise in the received signal.~~

This invention is based on ~~fundamentally~~ a substantially different principle of operation relying on; measurements of pulse lengths [spec.&2/p.8, cl.66] of incoming wave-form [spec. &7-8/p.5, &5/p.6]] with accuracy matching single gate delays [spec. &4/p.2, &1/p.3], and on digital processing of such accurate pulse lengths [spec. &1-5/p.6] in order to recover data transmitted by the wave-form or to analyze the waveform [spec. &3,&8,&9/p.1, &2/p.8].

Such superior principle of operation combined with adaptive signal processing algorithms utilizing verification of received waveforms [spec. &2-3/p.2, &4/p.7-&1/p.8], eliminate ~~all the above deficiencies~~ significant limitations of the prior art [spec. &1/p.2] and thus enable significantly longer transmission distances.

3. List of Citations ~~List~~ relevant to the Background of the Invention

Informations about such Citations communicated by the inventor during earlier prosecution stages, have been summarized in the "Summary of Background Art" attached to the Replay to the 2nd Office Action.

1. US 5,668,830 by Georgiu Christos, 16 September 1997
2. PCT/CA01/00723 / W0 01 91297 by Bogdan John, 29 November 2001
3. US 2002/0009171 by Ribo Jerome, 24 January 2002
4. US 5,592,125 by Williams Bertrand, 07 January 1997
5. US 6,987,817 by Reuveni David, 17 January 2006
6. US 4,977,582 by Zelle Bruce, 11 December 1990
7. US 5,467,464 by Oprescu Florin, 14 November 1995
8. US 5,872,791 by Propp David, 16 February 1999
9. EP 0 292 208 by American Telephone & Telegraph, 23 November 1988